library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity MUX8\_1 is

Port (i: in bit\_vector(7 downto 0);

s: in bit\_vector(2 downto 0);

y: out bit);

end MUX8\_1;

architecture Behavioral of MUX8\_1 is

begin

with s select

y <= i(0) when "000",

i(1) when "001",

i(2) when "010",

i(3) when "011",

i(4) when "100",

i(5) when "101",

i(6) when "110",

i(7) when "111";

end Behavioral;